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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,081	12/23/2003	Yoshiyuki Nagatomo	246940US2	8110

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EXAMINER	
NGUYEN, HOA CAO	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,081	NAGATOMO ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3 pages*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 2 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: The disclosed information that the **crystal particle** of copper having a **diameter** of 1.0 mm to 30 mm is questionable. The examiner assumes the diameter is in **μm** (micrometer) instead of **mm** (millimeter).

Appropriate correction is required.

Claim Objections

3. Claims 20-22 are objected to because of the following informalities:

As discussed above, the diameter "1.0mm - 30 mm" is questionable. The examiner assumes the diameter is in μm.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

These claims contain the Trademark "IACS" (International Annealed Copper Standard). This term should be replaced with the generic term for the material.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Ninomiya et al. (US 5981085).

Regarding claim 1, as shown in figure 3, Ninomiya et al. disclose a heat-conducting multilayer substrate comprising at least a copper circuitry layer (no number) of at least 99.999% purity and a ceramic layer 8 (substrate 8 is a alumina plate), see column 7, lines 45-51.

It is noticed that the alumina is known to be a material, which is a ceramic material, so it is ceramic layer. The ceramic layer 8 has copper layers on both sides which can be formed a wiring pattern, especially a wiring pattern that semiconductor device 7 is electrically connected to. Furthermore, Ninomiya et al. also disclose that a **circuit pattern can be formed** on the surface of an insulator substrate which isolates the device 7 from direct contact with the composite substrate 1 (a radiator or heat sink), see figure 3 and column 6, lines 59-67. In this case, substrate 8 is the insulator substrate.

The term copper includes any copper purity including the at least 99.999% purity. In other words, the at least 99.999% purity is within the limitation of the term copper. Furthermore, Ninomiya et al. disclose an example (test result) that copper particles of 99.99% purity were used during the test.

Regarding claim 2, as shown in figure 4, Ninomiya et al. disclose a heat-conducting multilayer substrate comprising:

(a) a ceramic layer 8, see claim 1 above;

(b) a copper circuitry layer having at least 99.999% purity provided on one side of the ceramic layer (the side where semiconductor device 7 connected to), see claim 1 above;

(c) a high-purity metal layer 9 (metal film of copper) provided on the other side of the ceramic layer, see column 8, lines 1-5.

Regarding claim 3, Ninomiya et al. disclose the metal layer 9, which can be copper and again the term copper includes any copper purity including the at least 99.999% purity, see column 8, lines 4-5.

Regarding claim 4, as shown in figure 4, Ninomiya et al. disclose a power module substrate comprising:

(a) an insulating substrate 8, see claim 1 above;

(b) a circuitry layer (no number, electrically connected to semiconductor device 7) laminated on one side (top side) of the insulating substrate 8, see claim 2 above;

(c) a metal layer 9 laminated on the other side of the insulating substrate, see claim 3 above;

(d) a semiconductor chip 7 loaded onto the circuitry layer by means of solder, see column 13, lines 17-20 (and it is also noticed that solder a chip onto a substrate is known in the art);

(e) a radiator 1 (composite substrate) joined to the metal layer; and

(f) the circuitry layer and the metal layer are composed of copper of at least 99.999% purity, see claims 2 and 3 above.

Regarding claim 5, Ninomiya et al. disclose the radiator 1 is joined to the metal layer 9 by solder, see column 8, lines 57-61.

Regarding claims 6 and 7, Ninomiya et al. disclose the insulating substrate is composed of alumina, which is Al_2O_3.

Regarding claims 8-13, Ninomiya et al. disclose every limitation as shown in claims 4-5 above and the limitation that (a) the circuitry layer and the metal layer release stress within 24 hours at 100°C and (b) elongation during rupture of the circuitry layer and the metal layer is from 20% to 30% within the range of -40°C to 150°C are interpreted to only require the ability to so perform.

In the case of product claim, only the structure of the claim distinguishes over the prior art.

Regarding claims 14-16, Ninomiya et al. disclose the thickness of the metal layer 11 (which is in the same manner as metal layer 9) is 0.5 mm. The thickness of the circuitry layer is within the workable ranges involves only routine skill in the art depending on the required electrical characteristic of an application. Furthermore, as an example, Ninomya et al. disclose that the thickness of layer 3 (see figure 1) is preferably selected according to the output of the semiconductor device 7, which is inherently also applied to the thickness of the circuitry layer, see column 5, lines 53-56.

Regarding claims 17-19, Ninomiya et al. disclose the conductivity of the circuitry layer and the metal layer is inherently at least 99% IACS, since the material is pure copper, see claim 1 above.

Regarding claims 20-22, Ninomiya et al. disclose every limitation as shown in claims 4-6 above and that the average particle diameter of crystalline particles of the circuitry layer and the metal layer is inherent properties, since the copper as taught by Ninomiya et al. includes a pure copper.

Citation of Related Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Circuit board, process for producing the same, and power module

Nagatomo et al. (US 20040022029) disclose a power module and power module with heat sink.

Nagase et al. (US 6033787) disclose a ceramic circuit board with heat sink.

Nagase et al. (US 20050214518) disclose a circuit board, process for producing the same, and power module.

Itoh (US 4926242) disclose an aluminum-silicon alloy heatsink for semiconductor devices.

Edwards (US 5881944) disclose a multi-layer solder seal band for semiconductor substrates.

Kabumoto et al. (US 5883428) disclose a package for housing a semiconductor element.

Toy et al. (US 5931222) disclose an adhesion promoting layer for bonding polymeric adhesive to metal and a heat sink assembly using same.

Ando et al. (US 6111322) disclose a semiconductor device and manufacturing method thereof.

Raleigh et al. (US 6300167) disclose a semiconductor device with flame sprayed heat spreading layer and method.

Mowatt et al. (US 6400573) disclose a multi-chip integrated circuit module.

Palanisamy et al. (US 6455930) disclose an integrated heat sinking packages using low temperature co-fired ceramic metal circuit board technology.

Chiu (US 6519154) discloses a thermal bus design to cool a microelectronic die.

Chiu et al. (US 6651736) disclose a short carbon fiber enhanced thermal grease.

O'Connor et al. (US 6667548) disclose a diamond heat spreading and cooling technique for integrated circuits.

Kikuchi et al. (US 6891247) disclose a semiconductor device including semiconductor bare chip mounted by flip-chip bonding, and board member with thin-film structure capacitor for semiconductor bare chip mounted by flip-chip bonding.

Ishikawa et al. (US 6911728) disclose a member for electronic circuit, method for manufacturing the member, and electronic part.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
2 December 2005

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